SEMICONDUCTOR MEMORY DEVICE AND METHOD OF OPERATION THEREOF

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device has a plurality of memory cells in an array, into which the memory cells data is writable, and which can subsequently be read. Each memory cell has a switching element with one terminal connected to a bit line of the array another terminal connected to at least one ferroelectric capacitor, and a control terminal connected to a word line. The cell may then be operated to detect the change in polarization of the ferroelectric capacitor when a voltage is applied which is not sufficient to cause a change of state of the ferroelectric capacitor. Alternatively, a ferroelectric capacitor and a capacitor other than a ferroelectric capacitor is connected to the switching element. In a further alternative, a plurality of ferroelectric capacitors are connected to the switching element, so that different data are writable into each.